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(72) Inventors:  
• Dünnebacke, Joachim, Ing.-grad.  
35745 Herborn (DE)  
• Schnabel, Steffen, Dipl.-Ing.  
35444 Bleibertal (DE)

(71) Applicant: Siemens Aktiengesellschaft  
80333 München (DE)

### (54) Hysteresis circuit

(57) Comparator circuit and voltage level detector comprising such comparator circuit including a first operational amplifier having a differential input, first and second voltage dividers being coupled to respectively a variable and a constant voltage source, outputs thereof being coupled to said differential input for supplying a differential input voltage thereto, the first operational amplifier having an output being coupled to its differential input and providing an output voltage stepwise var-

ying between first and second voltage levels at an inversion of the differential input voltage. In order to lower power consumption and increase the accuracy of level detection, one of the first and second voltage dividers is being provided with a stepwise variable voltage dividing factor, which is controlled by the output voltage of the first operational amplifier to increase the magnitude of said differential input voltage by a step value upon such inversion of the differential input voltage.

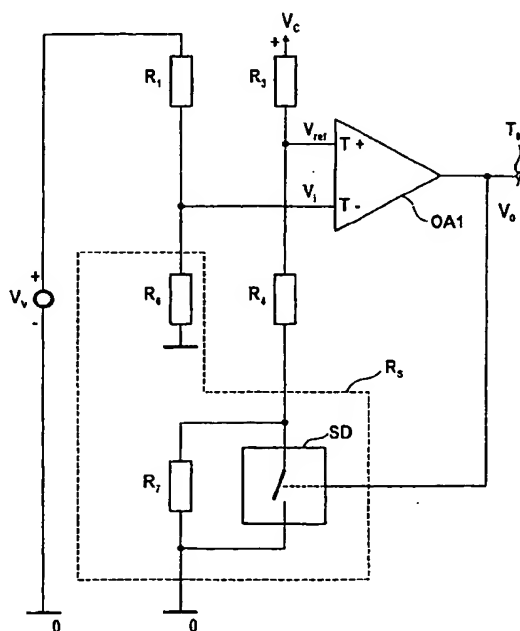


Fig. 3

## Description

[0001] The invention relates to a comparator circuit comprising a first operational amplifier having a differential input, first and second voltage dividers being coupled to respectively a variable and a constant voltage source, outputs thereof being coupled to said differential input for supplying a differential input voltage thereto, the first operational amplifier having an output being coupled to its differential input and providing an output voltage stepwise varying between first and second voltage levels at an inversion of the differential input voltage. Such comparator circuit is on itself known e.g. as Schmitt trigger, and is to compare an input voltage with a reference voltage, therewith operating as a voltage level detector.

[0002] Figure 1 illustrates a conventional comparator circuit. As shown therein, the comparator circuit includes an operational amplifier, hereinafter also referred to as first operational amplifier OA1, having a differential input comprising an inverting and a non-inverting input terminal, T- and T+ respectively. The inverting and non-inverting input terminals, T- and T+, are being supplied with an input voltage  $V_i$  and a reference voltage  $V_{ref}$  derived from a variable and a constant voltage source  $V_v$  and  $V_c$  through first and second voltage dividers, respectively. The first voltage divider comprises a serial arrangement of resistors R1 and R2, coupled between said variable voltage source  $V_v$  and mass, the common node of said resistors R1 and R2 constituting an output being coupled to the inverting input terminal T- of the operational amplifier OA1 to supply an input voltage  $V_i$  thereto. The second voltage divider comprises a serial arrangement of resistors R3 and R4, coupled between said constant voltage source  $V_c$  and mass, the common node of said resistors R3 and R4 constituting an output being coupled to the non-inverting input terminal T+ of the operational amplifier OA1 to supply a reference voltage  $V_{ref}$  thereto. The output voltage  $V_o$  of the operational amplifier OA1 is positively fed back from an output terminal  $T_o$  through a resistor R5 to its non-inverting input terminal T+, therewith obtaining a Schmitt-Trigger type circuit. As known, dependent on the polarity of the differential voltage ( $V_{ref}-V_i$ ) between its non-inverting and inverting input terminals, T+ and T-, hereinafter also being referred to as differential input voltage, the operational amplifier OA1 is switched between two stable states, in which it provides mutually different output voltage levels,  $V_{ol}$  and  $V_{oh}$ . Switching from one state to the other occurs when the polarity of the differential input voltage ( $V_{ref}-V_i$ ) reverses, i.e. at zero crossings of this differential input voltage ( $V_{ref}-V_i$ ). These zero crossings mark the occurrence of equal levels of both input voltage  $V_i$  and reference voltage  $V_{ref}$ . However, the above positive feedback causes the reference voltage  $V_{ref}$  to change stepwise at any zero crossing of the differential input voltage ( $V_{ref}-V_i$ ), therewith giving rise to an hysteresis response, which is inherent to Schmitt-Trigger type comparator circuits.

[0003] Figure 2 shows the transfer characteristic of the known comparator from the input voltage  $V_i$  to an output voltage  $V_o$  at its output terminal  $T_o$ . Suppose at a large negative value for the input voltage  $V_i$ , i.e. at a large positive value of the differential input voltage ( $V_{ref}-V_i$ ), the operational amplifier OA1 is in its first state providing a high level output voltage  $V_{oh}$ . A decrease of this large negative value of the input voltage  $V_i$ , causing said differential input voltage ( $V_{ref}-V_i$ ) to likewise decrease, does not change the state of the operational amplifier OA1, until this differential input voltage ( $V_{ref}-V_i$ ) crosses zero level, i.e. until this differential input voltage ( $V_{ref}-V_i$ ) reverses its polarity from positive into negative e.g. when the input voltage  $V_i$  crosses a first threshold level  $V_{t1}$ . Then the operational amplifier OA1 is switched into its second state providing a low level output voltage  $V_{ol}$ . Any further increase of the magnitude of the differential input voltage ( $V_{ref}-V_i$ ) in this negative polarity does not change the state of the operational amplifier OA1. If the input voltage  $V_i$  is subsequently decreased, causing the magnitude of the differential input voltage ( $V_{ref}-V_i$ ) to likewise decrease in said negative polarity, the operational amplifier OA1 returns from its second state into its first state, when the differential input voltage ( $V_{ref}-V_i$ ) reverses its polarity from negative to positive again, i.e. when said differential input voltage ( $V_{ref}-V_i$ ) crosses zero level again, i.e. at a second threshold level  $V_{t2}$ . Because of the above positive feedback of the output voltage  $V_{ol}$  of the operational amplifier to its non-inverting input terminal T+, said second threshold level  $V_{t2}$  lies below the first threshold level  $V_{t1}$ . Any further increase of the magnitude of the differential input voltage ( $V_{ref}-V_i$ ) in this positive polarity does not change the state of the operational amplifier OA1.

[0004] It is clear that the output voltage level of the operational amplifier OA1 is ambiguous with respect to said input voltage  $V_i$  for values of the input voltage  $V_i$  between the first and second threshold levels  $V_{t1}$  and  $V_{t2}$ . The narrower the hysteresis window, i.e. the range of the input voltage  $V_i$  between said first and second threshold levels  $V_{t1}$  and  $V_{t2}$ , the more accurate the comparator is in detecting the level of the input voltage.

[0005] To narrow the hysteresis window in this known comparator and therewith increase the accuracy of level detection, the value of the resistor R5 should be orders of magnitude greater than the value of the resistors R3 and R4 of the second voltage divider. However, to obtain limited power consumption, the resistors R3 and R4 have to be very large in themselves. In a practical embodiment the value of the resistors R3 and R4 are in the order of magnitude of 500 KOhm, whereas the resistor R5 is in the order of magnitude of some Mohm. In car applications, parasitic effects due to e.g. damp and/or corrosion, may effect the resistor R5 to dramatically reduce its resistance value, therewith strongly increasing the switching window.

[0006] It is an object of the invention to introduce a degree of freedom in a comparator circuit allowing to combine limited power consumption with robust and highly accurate level detection.

**[0007]** A comparator circuit comprising a first operational amplifier having a differential input, first and second voltage dividers being coupled to respectively a variable and a constant voltage source, outputs thereof being coupled to said differential input for supplying a differential input voltage thereto, the first operational amplifier having an output being coupled to its differential input and providing an output voltage stepwise varying between first and second voltage levels at an inversion of the differential input voltage, according to the invention is therefore characterized by one of the first and second voltage dividers having a stepwise variable voltage dividing factor being controlled by the output voltage of the first operational amplifier to increase the magnitude of said differential input voltage by a step value upon such inversion of the differential input voltage.

**[0008]** The invention is based on the recognition that separation of the features of zero crossing signalling and determination of the hysteresis window, which in the known comparator are combined in the feedback resistor R5, removes the necessity of applying such high ohmic feedback resistor and therewith increases the robustness and reliability of the circuit as a whole, and additionally introduces a degree of freedom allowing to optimise the voltage dividers with respect to minimum power consumption on the one hand and accuracy in level detection on the other hand. By applying the measure according to the invention the output voltage of the first operational amplifier, carrying zero crossing information, is used amongst others as a switching control signal for a stepwise increase of the differential input voltage in its actual polarity, i.e. in the polarity of the differential input voltage after the initiating zero crossing. As a result thereof, a differential input voltage changing at a zero crossing in polarity from negative to positive is being increased by said step value to a more positive value, a differential input voltage changing at a zero crossing in polarity from positive to negative is being increased by said step value to a more negative value. By an appropriate step value the hysteresis window can be set at any wanted value, i.e. sufficiently small to obtain an appropriate accuracy in level detection and sufficiently large to avoid unwanted jitter at a frequently changing level of the input voltage  $V_i$  around the reference voltage  $V_{ref}$ , from occurring.

**[0009]** Preferably, a comparator circuit according to the invention is characterized by said one of the first and second voltage dividers having a stepwise variable voltage dividing factor being constituted by a controlled voltage divider comprising a serial arrangement of a resistor and switched controlled resistor means, the common node thereof constituting an output of the controlled voltage divider, the switched controlled resistor means being controlled by the output voltage of the first operational amplifier to vary its resistance by a step value upon an inversion of the differential input voltage.

**[0010]** This measure allows to apply various alternative solutions for a stepwise increase of the differential input voltage at zero crossings of the differential input voltage of the operational amplifier in accordance with the invention

**[0011]** A first preferred embodiment of such comparator circuit is characterized in that the differential input of the first operational amplifier comprises an inverting and a non-inverting input terminal, the second voltage divider supplying a predetermined ratio of the output voltage of the constant voltage source to said non-inverting input terminal, the first voltage divider being constituted by said controlled voltage divider having said resistor and said switched controlled resistor means subsequently connected between the variable voltage source and mass, the output thereof being coupled to said inverting input terminal, the switched controlled resistor means being controlled by the output voltage of the first operational amplifier to increase its resistance by a step value upon an inversion of the differential input voltage caused by an increase of the voltage at the inverting input terminal above the voltage at the non-inverting input terminal.

**[0012]** By applying this measure, the input voltage at the inverting input terminal of the operational amplifier being defined by the voltage across the switched controlled resistor means, is increased by an increase of the resistance value of the switched controlled resistor means. A control thereof as mentioned above results in a stepwise increase of the differential input voltage at zero crossings of the differential input voltage of the operational amplifier in accordance with the invention.

**[0013]** A second preferred embodiment of a comparator circuit according to the invention is characterized in that the differential input of the first operational amplifier comprises an inverting and a non-inverting input terminal, the first voltage divider supplying a predetermined ratio of the output voltage of the variable voltage source to said inverting input terminal, the second voltage divider being constituted by said controlled voltage divider having said resistor and said switched controlled resistor means subsequently connected between the constant voltage source and mass, the output thereof being coupled to said non-inverting input terminal, the switched controlled resistor means being controlled by the output voltage of the first operational amplifier to decrease its resistance by a step value upon an inversion of the differential input voltage caused by an increase of the voltage at the inverting input terminal above the voltage at the non-inverting input terminal.

**[0014]** By applying this measure, the reference voltage at the non-inverting input terminal of the operational amplifier being defined by the voltage across the switched controlled resistor means, is decreased by a decrease in the resistance value of the switched controlled resistor means. A control thereof as mentioned above results in a stepwise increase of the differential input voltage at zero crossings of the differential input voltage of the operational amplifier in accordance with the invention.

**[0015]** A third preferred embodiment of a comparator circuit according to the invention is characterized in that the

**[0033]** The switched controlled resistor means  $R_s$  is being controlled by the output voltage of the first operational amplifier OA1 to increase its resistance by a step value upon an inversion of the differential input voltage ( $V_{ref}-V_i$ ) caused by an increase of the input voltage  $V_i$  above the reference voltage  $V_{ref}$ . For that purpose, the switched controlled resistor means  $R_s$  comprises a serial arrangement of a pair of resistors  $R_6$  and  $R_7$ , the resistor  $R_7$  being shunted by

a controllable switching device SD, which is controlled by the output voltage of the first operational amplifier OA1.

**[0034]** In the above first state, i.e. when the differential input voltage ( $V_{ref}-V_i$ ) has a positive value, i.e.  $V_i$  has a low value or equals mass potential, this output voltage attains a first voltage level, also being referred to as  $V_{oh}$ , setting the controllable switching device SD in closed position, therewith shortcircuiting  $R_7$ . The input voltage  $V_i$  is then defined by  $V_v \cdot R_6 / (R_1 + R_6)$ . An increase of the output voltage level of the variable voltage source  $V_v$  will cause the differential input voltage ( $V_{ref}-V_i$ ) to decrease and does not change the state of the first operational amplifier OA1 until  $V_i$  exceeds above  $V_{ref}$ , i.e. until the differential input voltage ( $V_{ref}-V_i$ ) crosses zero level and changes in polarity from positive to negative. At that point, the first operational amplifier OA1 is switched into its second state, providing an output voltage at a second voltage level, also being referred to as  $V_{ol}$ , switching the controllable switching device SD from closed to open position. As a result thereof, the resistor  $R_7$  is inserted in the serial arrangement of  $R_1$  and  $R_6$ , followed by a stepwise change in the voltage dividing factor of the first voltage divider from  $R_6 / (R_1 + R_6)$  to  $(R_6 + R_7) / (R_1 + R_6 + R_7)$ . This causes the input voltage level  $V_i$  to stepwise increase. The differential input voltage ( $V_{ref}-V_i$ ) therewith stepwise increases in the actual negative polarity. The voltage step value by which the differential input voltage ( $V_{ref}-V_i$ ) becomes more negative, is defined by the change in the dividing factor of the first voltage divider, i.e. by  $(R_6 + R_7) / (R_1 + R_6 + R_7) - R_6 / (R_1 + R_6)$ . The change in dividing factor therewith determines the width of the hysteresis window, i.e. the difference between the above first and second threshold levels  $V_{t1}$  and  $V_{t2}$ .

**[0035]** The use of the output voltage of the first operational amplifier as a switching control signal for changing the dividing factor of the first voltage divider by a step value, such that the differential input voltage ( $V_{ref}-V_i$ ) changing at a zero crossing in polarity from negative to positive is being increased by said step value to a more positive value, and the differential input voltage changing at a zero crossing in polarity from positive to negative is being increased by said step value to a more negative value, introduces a degree of freedom allowing to implement the features of zero crossing signalling and determination of the hysteresis window, which in the known comparator are combined in the feedback resistor  $R_5$ , separately. This makes it possible to optimise the comparator circuit with respect to minimum power consumption by an appropriate choice of the values of the resistors  $R_1$ ,  $R_6$  and  $R_7$  of the first voltage divider and  $R_3$ ,  $R_4$  of the second voltage divider, and independent therefrom to optimise the hysteresis window with regard to maximum accuracy in level detection on the one hand and stabilisation of the output voltage level against jitter at frequent variations of the input voltage level  $V_i$  around the reference voltage  $V_{ref}$ , on the other hand, by an appropriate ratio between the resistors  $R_1$ ,  $R_6$  and  $R_7$ .

**[0036]** In a practical implementation of this first preferred embodiment, the resistors  $R_1$ ,  $R_6$  and  $R_7$  of the first voltage divider and  $R_3$ ,  $R_4$  of the second voltage divider were chosen to be 560k $\Omega$ , 100k $\Omega$ , 18k $\Omega$  and 680k $\Omega$ , 220k $\Omega$ , respectively. The first operational amplifier was implemented with IC type LM324 and the controllable switching device with switching module type 74HCT4066. The constant voltage source had an output level voltage of 5 Volt.

**[0037]** Figure 4 shows a comparator circuit according to the invention in a second preferred embodiment, in which the outputs of the first and second voltage dividers are respectively coupled to the inverting and non-inverting input terminal  $T^-$  and  $T^+$  of the first operational amplifier OA1, and in a third preferred embodiment, in which the outputs of the first and second voltage dividers are coupled to said non-inverting and inverting input terminal  $T^+$  and  $T^-$ , respectively, as indicated by dotted lines.

**[0038]** Unlike the previously discussed first preferred embodiment, the first voltage divider in the second and third preferred embodiments comprises a serial arrangement of resistors  $R_1$  and  $R_2$  coupled between the variable voltage source  $V_v$  and mass and providing at its output an input voltage level  $V_i$  for the first operational amplifier OA1 being a predetermined ratio of the output voltage of the variable voltage source  $V_v$  as defined by the ratio of resistance values  $R_2 / (R_1 + R_2)$ . The second voltage divider is being constituted by a controlled voltage divider corresponding to the one used in the first preferred embodiment and having the resistor  $R_3$  and said switched controlled resistor means  $R_s$  serially connected between the constant voltage source  $V_c$  and mass. The output voltage of the second voltage divider provides the reference voltage level  $V_{ref}$  and is defined by the ratio of resistance values:  $R_3 / (R_3 + R_s)$ . The switched controlled resistor means  $R_s$  corresponds to the one used in the first preferred embodiment and comprises a serial arrangement of the resistors  $R_6$  and  $R_7$ , the resistor  $R_7$  being shunted by the controllable switching device SD and being controlled by the output voltage of the first operational amplifier OA1.

**[0039]** In the second preferred embodiment, the input voltage  $V_i$  and the reference voltage  $V_{ref}$  are being supplied to the inverting and non-inverting input terminal  $T^-$  and  $T^+$  of the first operational amplifier OA1, respectively. In the above first state, i.e. when the differential input voltage ( $V_{ref}-V_i$ ) has a high positive value, the output voltage  $V_o$  of the first operational amplifier OA1 attains the first voltage level, i.e.  $V_{oh}$ , setting the controllable switching device SD in open position. The input voltage  $V_i$  is then defined by  $V_v \cdot (R_6 + R_7) / (R_1 + R_6 + R_7)$ . A decrease of the output voltage level of the variable voltage source  $V_v$  will cause the differential input voltage ( $V_{ref}-V_i$ ) to likewise decrease and does not

change the state of the first operational amplifier OA1 until  $V_i$  exceeds above  $V_{ref}$ , i.e. until the differential input voltage ( $V_{ref}-V_i$ ) crosses zero level and changes in polarity from positive to negative. At that point, the first operational amplifier OA1 is switched into its second state, providing an output voltage  $V_o$  at the second voltage level  $V_{ol}$ , switching the controllable switching device SD from open to closed position. As a result thereof, the resistor R7 is shortcircuited, followed by a stepwise change in the voltage dividing factor of the second voltage divider from  $(R_6+R_7)/(R_1+R_6+R_7)$  to  $R_6/(R_1+R_6)$ . This causes the reference voltage level  $V_{ref}$  to stepwise decrease. The differential input voltage ( $V_{ref}-V_i$ ) therewith stepwise increases in the actual negative polarity. As in the first preferred embodiment, also here the voltage step value by which the differential input voltage ( $V_{ref}-V_i$ ) becomes more negative, is defined by the change in the dividing factor of the controlled voltage divider, in this second preferred embodiment being the second voltage divider, i.e. by  $(R_6+R_7)/(R_1+R_6+R_7) - R_6/(R_1+R_6)$ , defining the width of the hysteresis window. In this second preferred embodiment the width of the hysteresis window is fixed and does not vary with a varying input voltage  $V_i$ .

[0040] In the third preferred embodiment, the input voltage  $V_i$  and the reference voltage  $V_{ref}$  are being supplied to the non-inverting and inverting input terminal  $T_+$  and  $T_-$  of the first operational amplifier OA1, respectively, being indicated in Figure 4 by dotted lines as already mentioned above. The switched controlled resistor means  $R_s$  of the second voltage divider is being controlled by the output voltage  $V_o$  of the first operational amplifier OA1 to increase its resistance by a step value upon an inversion of the differential input voltage ( $V_{ref}-V_i$ ) caused by a decrease of the input voltage  $V_i$  below the reference voltage  $V_{ref}$  as will be described in more detail hereinafter.

[0041] When the input voltage  $V_i$  is highly positive, then the differential input voltage ( $V_{ref}-V_i$ ) is highly negative, setting the first operational amplifier OA1 in its second state. The output voltage  $V_o$  therewith attains the second voltage level  $V_{ol}$ , setting the controllable switching device SD in closed position. The reference voltage  $V_{ref}$  at the inverting input terminal  $T_-$  of the first operational amplifier OA1 is then defined by  $V_c \cdot R_6/(R_3+R_6)$ . A decrease of the output voltage level of the variable voltage source  $V_v$  will cause the differential input voltage ( $V_{ref}-V_i$ ) to likewise decrease and does not change the state of the first operational amplifier OA1 until the differential input voltage ( $V_{ref}-V_i$ ) crosses zero level and changes in polarity from negative to positive. At that point, the first operational amplifier OA1 is switched into its first state, providing an output voltage  $V_o$  at the first voltage level  $V_{oh}$ , switching the controllable switching device SD from closed to open position. As a result thereof, the resistor R7 is inserted in serial arrangement with the resistor R6. This causes the voltage dividing factor of the second voltage divider to increase stepwise from  $R_6/(R_3+R_6)$  to  $(R_6+R_7)/(R_3+R_6+R_7)$  and along therewith the reference voltage  $V_{ref}$ . The differential input voltage ( $V_{ref}-V_i$ ) therewith stepwise increases in the actual positive polarity. As in the first and second preferred embodiments, also here the voltage step value by which the differential input voltage ( $V_{ref}-V_i$ ) becomes more positive, is defined by the change in the dividing factor of the controlled voltage divider, in this third preferred embodiment being the second voltage divider, i.e. by  $(R_6+R_7)/(R_3+R_6+R_7) - R_6/(R_3+R_6)$  and defines the width of the hysteresis window. Also in this third preferred embodiment the width of the hysteresis window is fixed and does not vary with a varying input voltage  $V_i$ .

[0042] However, the output voltage  $V_o$  versus the input voltage  $V_i$  level variation of this third preferred embodiment is inverted with respect to the one in the first and second preferred embodiments.

[0043] In a practical implementation of this third preferred embodiment, the resistors R1 and R2 of the first voltage divider and R3, R6 and R7 of the second voltage divider were chosen to be 560k $\Omega$  and 100k $\Omega$ , 680k $\Omega$ , 220k $\Omega$  and 18k $\Omega$ , respectively. The first operational amplifier OA1 and the controllable switching device SD were implemented with IC type LM324 with switching module type 74HCT4066, respectively. The control of the switching module type 74HCT4066 by the output voltage  $V_o$  of the first operational amplifier OA1 had been reversed with respect to the one applied in the first preferred embodiment to set the controllable switching device SD in open position in the first state and in closed position in the second state. The constant voltage source  $V_c$  had an output level voltage of 5 Volt.

[0044] Figure 5 is a schematic diagram of a fourth preferred embodiment of a comparator circuit according to the invention, in which the second voltage divider comprises a serial arrangement of resistors R3 and R4 coupled between the constant voltage source  $V_c$  and mass, the common node of the resistors R3 and R4 providing an output of the second voltage divider supplying a fixed reference voltage  $V_{ref}$  to the non-inverting input terminal  $T_+$  of the first operational amplifier OA1,  $V_{ref}$  being a predetermined ratio  $R_4/(R_3+R_4)$  of the output voltage of the constant voltage source  $V_c$ .

[0045] The first voltage divider is a controlled voltage divider having a serial arrangement of switched controlled resistor means  $R_p$  and resistor R2 subsequently connected between the variable voltage source  $V_v$  and mass, the common node thereof providing an output of the second voltage divider and supplying a varying input voltage to the inverting input terminal  $T_-$  of the first operational amplifier OA1 being defined by  $V_v \cdot R_2/(R_p+R_2)$ . The switched controlled resistor means  $R_p$  comprises a resistor R8 being coupled in parallel to a serial arrangement of a further resistor R9 and a controllable switching device SD. In closed position of the controllable switching device SD, the resistance value of the switched controlled resistor means  $R_p$  is determined by the parallel connection of the resistors R8 and R9, i.e. by  $R_8 \cdot R_9/(R_8+R_9)$ . In opened position of the controllable switching device SD, the resistance value of the switched controlled resistor means  $R_p$  is determined by the resistor R8, which is greater than the resistance value in closed position by the resistance step value  $R_8 - R_8 \cdot R_9/(R_8+R_9)$ , hereinafter being referred to as  $\Delta R_p$ .

[0046] The switched controlled resistor means  $R_p$  is being controlled by the output voltage of the first operational amplifier OA1 to decrease its resistance by a step value upon an inversion of the differential input voltage ( $V_{ref}-V_i$ ) caused by an increase of the input voltage  $V_i$  above the reference voltage  $V_{ref}$ . As explained above this is obtained by switching the controllable switching device SD from opened to closed position.

[0047] In the first state of the first operational amplifier OA1 occurring when the differential input voltage ( $V_{ref}-V_i$ ) has a high positive value, this output voltage attains a first voltage level, i.e.  $V_{oh}$ , setting the controllable switching device SD in open position, therewith inactivating the resistor R9. The input voltage  $V_i$  is then defined by  $V_v \cdot R_2 / (R_2 + R_8)$ . An increase of the output voltage level of the variable voltage source  $V_v$  will cause the differential input voltage ( $V_{ref}-V_i$ ) to decrease and does not change the state of the first operational amplifier OA1 until  $V_i$  exceeds above  $V_{ref}$ , i.e. until the differential input voltage ( $V_{ref}-V_i$ ) crosses zero level and changes in polarity from positive to negative. At that point, the first operational amplifier OA1 is switched into its second state, providing an output voltage at a second voltage level, e.g.  $V_{ol}$ , switching the controllable switching device SD from open to closed position. As a result thereof, the resistor R9 is being connected in parallel to the resistor R8, followed by a stepwise increase in the voltage dividing factor of the first voltage divider by  $R_2 / (R_2 + R_8 + \Delta R_p)$ . This causes the input voltage level  $V_i$  to stepwise increase with the same factor. Along therewith, the differential input voltage ( $V_{ref}-V_i$ ) increases in the actual negative polarity by a voltage step value defined by said increase in the voltage dividing factor of the first voltage divider, i.e. by  $V_v \cdot R_2 / (R_2 + R_8 + \Delta R_p)$ . This step voltage value is defined by the ratio in resistance values of the resistors R2, R8 and R9 and in its turn determines the width of the hysteresis window, i.e. the difference between the above first and second threshold levels  $V_{t1}$  and  $V_{t2}$ . An implementation of the first operational amplifier OA1 by means of IC type LM 324 and switching device SD by means of switching module type 74HCT4066 requires an inverter device (not shown) to be inserted between such first operational amplifier OA1 and such switching device SD.

[0048] Figure 6 is a schematic diagram of a fifth preferred embodiment of a comparator circuit according to the invention, in which the first voltage divider comprises a serial arrangement of resistors R1 and R2 coupled between the variable voltage source  $V_v$  and mass. The common node of the resistors R1 and R2 provides an output of this first voltage divider supplying a variable input voltage  $V_i$  to the inverting input terminal T- of the first operational amplifier OA1, being a predetermined ratio  $R_2 / (R_1 + R_2)$  of the output voltage of the variable voltage source  $V_v$ . The second voltage divider is a controlled voltage divider having a serial arrangement of switched controlled resistor means  $R_p$  and resistor R4 subsequently connected between the constant voltage source  $V_c$  and mass, the common node thereof providing an output of the second voltage divider and supplying a reference voltage  $V_{ref}$  to the non-inverting input terminal T+ of the first operational amplifier OA1 being defined by  $V_c \cdot R_4 / (R_p + R_4)$ . Also here, the resistance value of the switched controlled resistor means  $R_p$  decreases at the closing of the switching device SD by a stepvalue of  $\Delta R_p$ .

[0049] In this fifth preferred embodiment, the switched controlled resistor means  $R_p$  is being controlled by the output voltage  $V_o$  of the first operational amplifier OA1 to increase its resistance by the above step value upon an inversion of the differential input voltage ( $V_{ref}-V_i$ ) caused by an increase of the input voltage  $V_i$  above the reference voltage  $V_{ref}$ , as will be explained in more detail hereinafter.

[0050] In the above state of the first operational amplifier OA1, i.e. when the differential input voltage ( $V_{ref}-V_i$ ) has a high positive value, the output voltage  $V_o$  of the first operational amplifier OA1 attains the first voltage level, e.g.  $V_{oh}$ , setting the controllable switching device SD in closed position. The reference voltage  $V_{ref}$  is then defined by  $V_c \cdot R_4 / (R_4 + (R_8 \cdot R_9 / (R_8 + R_9)))$ . An increase of the output voltage level of the variable voltage source  $V_v$  will cause the differential input voltage ( $V_{ref}-V_i$ ) to decrease and does not change the state of the first operational amplifier OA1 until  $V_i$  exceeds above  $V_{ref}$ , i.e. until the differential input voltage ( $V_{ref}-V_i$ ) crosses zero level and changes in polarity from positive to negative. At that point, the first operational amplifier OA1 is switched into its second state, providing an output voltage  $V_o$  at the second voltage level  $V_{ol}$ , switching the controllable switching device SD from closed to open position. As a result thereof, the resistor R9 is inactivated, followed by a stepwise decrease in the voltage dividing factor of the second voltage divider from  $R_4 / (R_4 + (R_8 \cdot R_9 / (R_8 + R_9)))$  to  $R_4 / (R_4 + R_8)$ . This causes the reference voltage level  $V_{ref}$  to stepwise decrease too. Along therewith, the differential input voltage ( $V_{ref}-V_i$ ) increases in the actual negative polarity by a voltage step value defined by said decrease in the voltage dividing factor of the second voltage divider, i.e. by  $V_c \cdot R_4 / (R_4 + R_8 + \Delta R_p)$ . This step voltage value is defined by the ratio in resistance values of the resistors R4, R8 and R9 and in its turn determines the width of the hysteresis window, i.e. the difference between the above first and second threshold levels  $V_{t1}$  and  $V_{t2}$ . In this fifth preferred embodiment the width of the hysteresis window is fixed and does not vary with a varying input voltage  $V_i$ .

[0051] Figure 7 is a schematic diagram of a sixth preferred embodiment of a comparator circuit according to the invention in which the second voltage divider comprises a serial arrangement of resistors R3 and R4 coupled between the constant voltage source  $V_c$  and mass, the common node of the resistors R3 and R4 providing an output of the second voltage divider supplying a fixed reference voltage  $V_{ref}$  to the non-inverting input terminal T+ of the first operational amplifier OA1,  $V_{ref}$  being a predetermined ratio  $R_4 / (R_3 + R_4)$  of the output voltage of the constant voltage source  $V_c$ .

[0052] The first voltage divider is a controlled voltage divider having a serial arrangement of resistor R2 and switched

controlled resistor means  $R_p$  subsequently connected between the variable voltage source  $V_v$  and mass, the common node thereof providing an output of the second voltage divider and supplying a varying input voltage  $V_i$  to the inverting input terminal T- of the first operational amplifier OA1 being defined by  $V_v \cdot R_2 / (R_p + R_2)$ . The switched controlled resistor means  $R_p$  comprises resistor  $R_8$  being coupled in parallel to a serial arrangement of resistor  $R_9$  and a controllable switching device SD. In closed position of the controllable switching device SD, the resistance value of the switched controlled resistor means  $R_p$  is determined by the parallel connection of the resistors  $R_8$  and  $R_9$ , i.e. by  $R_8 \cdot R_9 / (R_8 + R_9)$ . In opened position of the controllable switching device SD, the resistance value of the switched controlled resistor means  $R_p$  is determined by the resistor  $R_8$ , which is greater than the resistance value in closed position by the resistance step value  $R_8 - R_8 \cdot R_9 / (R_8 + R_9)$ , hereinafter being referred to as  $\Delta R_p$ . The resistance step value  $\Delta R_p$  determines the width of the hysteresis window.

[0053] The switched controlled resistor means  $R_p$  is being controlled by the output voltage of the first operational amplifier OA1 to decrease its resistance by a step value upon an inversion of the differential input voltage ( $V_{ref} - V_i$ ) caused by an increase of the input voltage  $V_i$  above the reference voltage  $V_{ref}$ . As explained above this is obtained by the first operational amplifier OA1 switching the controllable switching device SD from closed to opened position.

[0054] In a practical implementation of this sixth preferred embodiment, the resistor  $R_1$  of the first voltage divider and  $R_3$  and  $R_4$  of the second voltage divider were chosen to be 560k $\Omega$ , 680k $\Omega$  and 220k $\Omega$ , respectively. The resistors  $R_8$  and  $R_9$  of the switched controlled resistor means  $R_p$  were chosen to be 100k $\Omega$  and 1M $\Omega$ , respectively. The first operational amplifier OA1 and the controllable switching device SD were implemented with IC type LM324 with switching module type 74HCT4066, respectively.

[0055] Figure 8 shows a comparator circuit according to the invention in a seventh preferred embodiment, in which the outputs of the first and second voltage dividers are respectively coupled to the non-inverting and inverting input terminals T+ and T- of the first operational amplifier OA1. The first and second voltage dividers are constituted by first and second controlled voltage dividers, respectively. The first voltage divider comprises the above resistor  $R_1$  and first switched controlled resistor means  $R_{s1}$ , subsequently connected in series between the variable voltage source  $V_v$  and mass. The second voltage divider comprises second switched controlled resistor means  $R_{s2}$ , and a resistor  $R_4$  subsequently connected in series between the constant voltage source  $V_c$  and mass supplying a predetermined ratio of the output voltage of the constant voltage source ( $V_c$ ) to said inverting input terminal (T-). Both first and second switched controlled resistor means  $R_{s1}$  and  $R_{s2}$  correspond in circuitry to the above switched controlled resistor means  $R_s$ . The first switched controlled resistor means  $R_{s1}$  comprises a serial arrangement of resistors  $R_6$  and  $R_7$ , the resistor  $R_7$  being shunted by the controlled switching device SD. The second switched controlled resistor means  $R_{s2}$  comprises a serial arrangement of resistors  $R_6'$  and  $R_7'$ , the resistor  $R_7'$  being shunted by the controlled switching device SD'. Upon an inversion of the differential input voltage ( $V_i - V_{ref}$ ) from positive to negative polarity caused by a decrease of the voltage  $V_i$  at the non-inverting input terminal T+ below the voltage  $V_{ref}$  at the inverting input terminal T-, the output voltage of the first operational amplifier OA1 causes the controlled switching devices SD and SD' to simultaneously shortcircuit resistors  $R_7$  and  $R_7'$ . As a result thereof differential input voltage ( $V_i - V_{ref}$ ) increase in negative polarity, i.e. becomes more negative, by a step value defining the hysteresis window. Dependent on the polarity of the various signals the use of inverters may be necessary to obtain the above functioning of the comparator in accordance with the invention.

[0056] Figure 9 is a schematic diagram of a eighth preferred embodiment of a comparator circuit according to the invention comprising a cascade of first to fourth operational amplifiers OA1-OA4, the above mentioned first and second voltage dividers in common, the first voltage divider comprising a serial arrangement of first to ninth resistors  $r_1$  to  $r_9$  subsequently coupled between the variable voltage source  $V_v$  and mass and having first to eighth outputs O1-O8 at the subsequent nodes between said resistors  $r_1$ - $r_9$ . The first to fourth outputs O1-O4 are coupled to the inverting inputs T- of the first to fourth operational amplifiers OA1-OA4, respectively. The fifth to eighth outputs O5-O8 are shunted through first to fourth controllable switching devices SD1-SD4, respectively, to mass. The second voltage divider comprises resistors  $R_3$  and  $R_4$  being serially coupled between the constant voltage source  $V_c$  and mass, supplying a reference voltage  $V_{ref}$  to the non-inverting input terminals T+ of each of the first to fourth operational amplifiers OA1-OA4, this reference voltage  $V_{ref}$  corresponding to  $V_c \cdot R_4 / (R_3 + R_4)$ . This sixth preferred embodiment a comparator circuit according to the invention provides a 4-level detection of a varying input voltage  $V_i$ , as will be described in more detail hereinafter.

[0057] If the differential input voltage ( $V_{ref} - V_i$ ) has a high positive value, the operational amplifiers OA1-OA4 will assume the above first state and provide an output voltage at the above first voltage level, e.g.  $V_{oh}$ , setting the controllable switching devices SD1-SD4 in closed position, therewith shortcircuiting  $r_6$ - $r_9$ . The input voltages  $V_{i1}$  to  $V_{i4}$  of the operational amplifiers OA1-OA4 are then respectively defined by  $V_v \cdot (r_2 + r_3 + r_4 + r_5) / (r_1 + r_2 + r_3 + r_4 + r_5)$ ;  $V_v \cdot (r_3 + r_4 + r_5) / (r_1 + r_2 + r_3 + r_4 + r_5)$ ;  $V_v \cdot (r_4 + r_5) / (r_1 + r_2 + r_3 + r_4 + r_5)$ ;  $V_v \cdot r_5 / (r_1 + r_2 + r_3 + r_4 + r_5)$ . An increase of the output voltage level of the variable voltage source  $V_v$  will cause the differential input voltages ( $V_{ref} - V_{i1}$ ) to ( $V_{ref} - V_{i4}$ ) of the operational amplifiers OA1-OA4 to decrease and does not change the state of any of these operational amplifiers until  $V_{i1}$  exceeds above  $V_{ref}$ , i.e. until the differential input voltage ( $V_{ref} - V_{i1}$ ) of the first operational amplifiers OA1 crosses zero level and



changes in polarity from positive to negative. At that point, the first operational amplifier OA1 is switched into its second state, providing an output voltage  $V_{o1}$  at the second voltage level, e.g.  $V_{o1}$ , switching the controllable switching device SD1 from closed to open position. As a result thereof, the resistor  $r_6$  is inserted in the serial arrangement of  $r_1$  to  $r_5$ , followed by a stepwise change in the voltage dividing factor of the first voltage divider at the outputs O1-O4 from

$$(r_2+r_3+r_4+r_5)/(r_1+r_2+r_3+r_4+r_5); (r_3+r_4+r_5)/(r_1+r_2+r_3+r_4+r_5); (r_4+r_5)/(r_1+r_2+r_3+r_4+r_5) \text{ and } r_5/(r_1+r_2+r_3+r_4+r_5) \text{ to } (r_2+r_3+r_4+r_5+r_6)/(r_1+r_2+r_3+r_4+r_5+r_6); (r_3+r_4+r_5+r_6)/(r_1+r_2+r_3+r_4+r_5+r_6); (r_4+r_5+r_6)/(r_1+r_2+r_3+r_4+r_5+r_6) \text{ and } (r_5+r_6)/(r_1+r_2+r_3+r_4+r_5+r_6).$$

This causes the input voltages  $V_{i1}$  to  $V_{i4}$  to stepwise increase. The differential input voltage ( $V_{ref}-V_{i1}$ ) therewith stepwise increases in the actual negative polarity. The voltage step value by which the differential input voltage ( $V_{ref}-V_{i1}$ ) becomes more negative, is defined by the change in the dividing factor of the first voltage divider and corresponds to  $V_v \cdot (r_2+r_3+r_4+r_5+r_6)/(r_1+r_2+r_3+r_4+r_5+r_6) - V_v \cdot (r_2+r_3+r_4+r_5)/(r_1+r_2+r_3+r_4+r_5)$ . This voltage step value determines the width of the hysteresis window of the first operational amplifier OA1.

**[0058]** A further increase of the output voltage level of the variable voltage source  $V_v$  does not change the second state of the operational amplifiers OA1 and the first state of the operational amplifiers OA2-OA4 until  $V_{i2}$  exceeds above  $V_{ref}$ , i.e. until the differential input voltage ( $V_{ref}-V_{i1}$ ) of the second operational amplifiers OA2 crosses zero level and changes in polarity from positive to negative. At that point, the second operational amplifier OA2 is switched into its second state, providing an output voltage  $V_{o2}$  at the second voltage level  $V_{o1}$ , switching the controllable switching device SD2 from closed to open position. As a result thereof, the resistor  $r_7$  is inserted in the serial arrangement of  $r_1$  to  $r_6$ , followed by a stepwise change in the voltage dividing factor of the first voltage divider at the outputs O1-O4 from

$$(r_2+r_3+r_4+r_5+r_6)/(r_1+r_2+r_3+r_4+r_5+r_6); (r_3+r_4+r_5+r_6)/(r_1+r_2+r_3+r_4+r_5+r_6); (r_4+r_5+r_6)/(r_1+r_2+r_3+r_4+r_5+r_6) \text{ and } (r_5+r_6)/(r_1+r_2+r_3+r_4+r_5+r_6) \text{ to } (r_2+r_3+r_4+r_5+r_6+r_7)/(r_1+r_2+r_3+r_4+r_5+r_6+r_7); (r_3+r_4+r_5+r_6+r_7)/(r_1+r_2+r_3+r_4+r_5+r_6+r_7); (r_4+r_5+r_6+r_7)/(r_1+r_2+r_3+r_4+r_5+r_6+r_7) \text{ and } (r_5+r_6+r_7)/(r_1+r_2+r_3+r_4+r_5+r_6+r_7).$$

This causes the input voltages  $V_{i1}$  to  $V_{i4}$  to stepwise increase. The differential input voltage ( $V_{ref}-V_{i2}$ ) therewith stepwise increases in the actual negative polarity. The voltage step value by which the differential input voltage ( $V_{ref}-V_{i2}$ ) becomes more negative, is defined by the change in the dividing factor of the first voltage divider and corresponds to  $V_v \cdot (r_3+r_4+r_5+r_6+r_7)/(r_1+r_2+r_3+r_4+r_5+r_6+r_7) - V_v \cdot (r_3+r_4+r_5+r_6)/(r_1+r_2+r_3+r_4+r_5+r_6)$ . This voltage step value determines the width of the hysteresis window of the second operational amplifier OA2.

**[0059]** The change of state of the operational amplifiers OA3 and OA4 follow in likewise manner upon a further increase of the output voltage level of the variable voltage source  $V_v$ .

**[0060]** Starting from a situation in which the operational amplifiers OA1-OA4 all are in the second state, a decrease of the output voltage level of the variable voltage source  $V_v$ , i.e. an decrease of the differential input voltages ( $V_{ref}-V_{i1}$ ) to ( $V_{ref}-V_{i4}$ ) will first cause the state of the fourth operational amplifier OA4 to return from the second state into the first state, followed at a further decrease of the output voltage level of the variable voltage source  $V_v$ , i.e. a further decrease of the differential input voltages ( $V_{ref}-V_{i1}$ ) to ( $V_{ref}-V_{i4}$ ), by the return of the third operational amplifier OA3 from the second into the first state, and so forth and so on.

**[0061]** By a proper choice of the values of the resistances  $r_1$ - $r_9$  four voltage detection levels can be obtained, evenly spread over the full input voltage variation range, while limiting power consumption. Unlike the above discussed preferred embodiments, where an input voltage  $V_i$  is compared with one single detection or voltage reference level and is differentiated into two voltage ranges (either below or above said voltage reference level  $V_{ref}$ ), this sixth preferred embodiment provides a differentiation of the input voltage  $V_i$  into five subsequent voltage ranges, reflected in the output voltages  $V_{o1}$ - $V_{o4}$  of the operational amplifiers OA1-OA4 and allowing for a more refined measuring of the level of the input voltage  $V_i$ .

**[0062]** By extending the number of operational amplifiers to in the cascade to  $n$ , the number of serially arranged resistors in the first voltage divider to  $(2n+1)$  and controllable switching devices to  $n$ , a differentiation of the input voltage  $V_i$  into  $n+1$  subsequent voltage ranges is obtained.

**[0063]** Figure 10a shows a bipolar NPN transistor as a first alternative embodiment of the controlled switching device SD, having its base electrode coupled via a base resistor  $R_{base}$  to the output of the first operational amplifier OA1. If used in the switched controlled resistor means  $R_s$ , then the collector-emitter path thereof is being shunted across the resistor  $R_7$ . If used in the switched controlled resistor means  $R_p$ , then the collector-emitter path thereof is being serially connected to the resistor  $R_9$ . In case of the use of the controlled switching device SD for switching through to the positive supply voltage a PNP transistor is to be used instead of the above NPN transistor.

**[0064]** Figure 10b shows a field effect CMOS transistor type BST82 as a second alternative embodiment of the controlled switching device SD, having its gate electrode coupled to the output of the first operational OA1. If used in the switched controlled resistor means  $R_s$ , then the drain-source path thereof is being shunted across the resistor  $R_7$ . If used in the switched controlled resistor means  $R_p$ , then the drain-source path thereof is being serially connected to the resistor  $R_9$ . In case of the use of the controlled switching device SD for switching through to the positive supply voltage a p-channel MOSFET has to be used instead of the above CMOS transistor type BST82, which is an n-channel MOSFET type.

**[0065]** The comparator according to the invention in the above preferred embodiments is generally applicable, how-



ever, is in particular suitable for use in car applications, such as a voltage detector providing e.g. an alert signal if the battery voltage is low or some crucial car feature needs servicing. In such application, improvement in the accuracy of level detection is obtained by a stabilisation of the constant and/or the variable voltage source and/or the output voltages of the first and second voltage dividers against temperature variations (not shown) and/or by an integration of interference pulses on the output voltage of both voltage sources (not shown). The implementation of these improvements are within the knowledge of the skilled man and needs no further amplification.

[0066] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

[0067] For instance, the use of the output voltage of the first operational amplifier OA1 as a switching control signal may necessitate to use inverters, switched controlled resistor means may be substituted for one or more of the resistors R1-R4 of the first and second voltage dividers, other than shown in the Figures, with an adequate adaptation the outputs of the first and second voltage dividers in the embodiments shown may well be coupled to the differential input of the operational amplifier opposite to the coupling shown, switched controlled resistor means Rs used in the first to third preferred embodiments may well be replaced by the switched controlled resistor means Rp of the fourth and fifth preferred embodiments and vice versa. Furthermore, the measure to invert the input voltage Vi versus output voltage Vo characteristic of the comparator as illustrated by way of example in the third preferred embodiment, may well be applied to the other preferred embodiments for the same purpose.

## Claims

1. Comparator circuit comprising a first operational amplifier (OA1) having a differential input (T+, T-), first and second voltage dividers being coupled to respectively a variable and a constant voltage source (Vv, Vc), outputs thereof being coupled to said differential input (T+, T-) for supplying a differential input voltage (Vref-Vi) thereto, the first operational amplifier (OA1) having an output (Vo) being coupled to its differential input (T+, T-) and providing an output voltage (Vo) stepwise varying between first and second voltage levels at an inversion of the differential input voltage (Vref-Vi), **characterised by** one of the first and second voltage dividers having a stepwise variable voltage dividing factor being controlled by the output voltage of the first operational amplifier (OA1) to increase the magnitude of said differential input voltage (Vref-Vi) by a step value upon such inversion of the differential input voltage (Vref-Vi).
2. Comparator circuit according to claim 1, **characterised by** said one of the first and second voltage dividers having a stepwise variable voltage dividing factor being constituted by a controlled voltage divider comprising a serial arrangement of a resistor (R1-R4) and switched controlled resistor means (Rs, Rp), the common node thereof constituting an output of the controlled voltage divider, the switched controlled resistor means (Rs, Rp) being controlled by the output voltage (Vo) of the first operational amplifier (OA1) to vary its resistance by a step value upon an inversion of the differential input voltage (Vref-Vi).
3. Comparator circuit according to claim 2, **characterised in that** the differential input (T+, T-) of the first operational amplifier (OA1) comprises an inverting (T-) and a non-inverting (T+) input terminal, the second voltage divider supplying a predetermined ratio of the output voltage of the constant voltage source (Vv) to said non-inverting input terminal (T+), the first voltage divider being constituted by said controlled voltage divider having said resistor (R1) and said switched controlled resistor means (Rs) subsequently connected between the variable voltage source (Vv) and mass, the output thereof being coupled to said inverting input terminal (T-), the switched controlled resistor means (Rs) being controlled by the output voltage of the first operational amplifier to increase its resistance by a step value upon an inversion of the differential input voltage (Vref-Vi) caused by an increase of the voltage (Vi) at the inverting input terminal (T-) above the voltage (Vref) at the non-inverting input terminal (T+).
4. Comparator circuit according to claim 2, **characterised in that** the differential input (T+, T-) of the first operational amplifier (OA1) comprises an inverting (T-) and a non-inverting input terminal (T+), the first voltage divider supplying a predetermined ratio of the output voltage of the variable voltage source (Vv) to said inverting input terminal (T-), the second voltage divider being constituted by said controlled voltage divider having said resistor (R3) and said switched controlled resistor means (Rs) subsequently connected between the constant voltage source (Vc) and mass, the output thereof being coupled to said non-inverting input terminal (T+), the switched controlled resistor means (Rs) being controlled by the output voltage (Vo) of the first operational amplifier (OA1) to decrease its resistance by a step value upon an inversion of the differential input voltage (Vref-Vi) caused by an increase of the voltage at the inverting input terminal (Vi) above the voltage at the non-inverting input terminal (Vref).

5. Comparator circuit according to claim 2, **characterised in that** the differential input (T+, T-) of the first operational amplifier (OA1) comprises an inverting (T-) and a non-inverting (T+) input terminal, the second voltage divider supplying a predetermined ratio of the output voltage of the constant voltage source (Vc) to said non-inverting input terminal (T+), the first voltage divider being constituted by said controlled voltage divider having said switched controlled resistor means (Rp) and said resistor (R2) subsequently connected between the variable voltage source (Vv) and mass, the output thereof being coupled to said inverting input terminal (T-), the switched controlled resistor means (Rp) being controlled by the output voltage (Vo) of the first operational amplifier (OA1) to decrease its resistance by a step value upon an inversion of the differential input voltage (Vref-Vi) caused by an increase of the voltage at the inverting input terminal (Vi) above the voltage at the non-inverting input terminal (Vref).
6. Comparator circuit according to claim 2, **characterised in that** the differential input (T+, T-) of the first operational amplifier (OA1) comprises an inverting (T-) and a non-inverting (T+) input terminal, the first voltage divider supplying a predetermined ratio of the output voltage of the variable voltage source (Vv) to said inverting input terminal (T-), the second voltage divider being constituted by said controlled voltage divider having said switched controlled resistor means (Rp) and said resistor (R4) subsequently connected between the constant voltage source (Vc) and mass, the output thereof being coupled to said non-inverting input terminal (T+), the switched controlled resistor means (Rp) being controlled by the output voltage (Vo) of the first operational amplifier (OA1) to increase its resistance by a step value upon an inversion of the differential input voltage (Vref-Vi) caused by an increase of the voltage at the inverting input terminal (Vi) above the voltage at the non-inverting input terminal (Vref).
7. Comparator circuit according to claim 2, **characterised in that** the differential input (T+, T-) of the first operational amplifier (OA1) comprises an inverting (T-) and a non-inverting (T+) input terminal, the first voltage divider supplying a predetermined ratio of the output voltage of the variable voltage source (Vv) to said non-inverting input terminal (T+), the second voltage divider being constituted by said controlled voltage divider having said resistor (R3) and said switched controlled resistor means (Rp) subsequently connected between the constant voltage source (Vc) and mass, the output thereof being coupled to said inverting input terminal (T-), the switched controlled resistor means (Rp) being controlled by the output voltage (Vo) of the first operational amplifier (OA1) to increase its resistance by a step value upon an inversion of the differential input voltage (Vref-Vi) caused by a decrease of the voltage at the non-inverting input terminal (Vi) below the voltage at the inverting input terminal (Vref).
8. Comparator circuit according to claim 2, **characterised in that** the differential input (T+, T-) of the first operational amplifier (OA1) comprises an inverting (T-) and a non-inverting (T+) input terminal, the first voltage divider being constituted by a first controlled voltage divider having a resistor (R1) and first switched controlled resistor means (Rs1) subsequently connected between the variable voltage source (Vv) and mass, the output thereof being coupled to said non-inverting input terminal (T+), the second voltage divider being constituted by a second controlled voltage divider having second switched controlled resistor means (Rs2) and a resistor (R4) subsequently connected between the constant voltage source (Vc) and mass supplying a predetermined ratio of the output voltage of the constant voltage source (Vc) to said inverting input terminal (T-), the first and second switched controlled resistor means (Rs1 and Rs2) being controlled by the output voltage of the first operational amplifier to decrease their resistance by a step value upon an inversion of the differential input voltage (Vi-Vref) caused by an decrease of the voltage (Vi) at the non-inverting input terminal (T+) below the voltage (Vref) at the inverting input terminal (T-).
9. Comparator circuit according to one of claims 2 to 8, **characterised in that** said switched controlled resistor means (Rs) comprises a serial arrangement of a pair of resistors (R6, R7, R6', R7'), one of which (R7, R7') being shunted by a controllable switching device (SD).
10. Comparator circuit according to one of claims 2 to 8, **characterised in that** said switched controlled resistor means (Rp) comprises a resistor (R8) coupled in parallel to a serial arrangement of a further resistor (R9) and a controllable switching device (SD).
11. Comparator circuit according to one of claims 2 to 4, **characterized by** said cascade of n operational amplifiers (OA1-OAn) including said first operational amplifier (OA1) having said first and second voltage dividers in common, the first voltage divider comprising a serial arrangement of first to (2n+1)<sup>th</sup> resistors (r1-r2n+1) subsequently coupled between the variable voltage source (Vv) and mass and having first to 2n<sup>th</sup> outputs (O1-O2n) at the subsequent nodes between said resistors (r1-r2n+1), the first to n<sup>th</sup> outputs (O1-On) of the second voltage divider being coupled to the inverting inputs (T-) of the first to n<sup>th</sup> operational amplifiers (OA1-Oan), respectively, the (n+1)<sup>th</sup> to 2n<sup>th</sup> outputs (On+1-O2n) being shunted through first to n<sup>th</sup> controllable switching devices (SD1-SDn), respectively, to mass, the second voltage divider supplying a predetermined ratio of the output voltage of the constant voltage source

(Vref) to the non-inverting input terminals (T+) of each operational amplifier (OA1-OAn).

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12. Comparator circuit according to one of claims 9 to 11, **characterised in that** each said switching device (SD, SD1-SDn) comprises a switching transistor (FET1) implemented in MOS technology.
13. Comparator circuit according to one of claims 9 to 11, **characterised in that** each said switching device (SD, SD1-SDn) comprises a bipolar switching transistor (Tr).
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14. Comparator circuit according to one of claims 9 to 11, **characterised in that** each said switching device (SD, SD1-SDn) comprises a transistor (FET2) implemented in MOS technology.
15. Voltage level detector comprising a comparator circuit according to one of claims 1 to 14, **characterised in that** the constant voltage source (Vc) is temperature stabilised.
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16. Voltage level detector according to claim 15, **characterised by** an integration of interference pulses on the output voltage of both voltage dividers (Vref, Vi1-Vi4).

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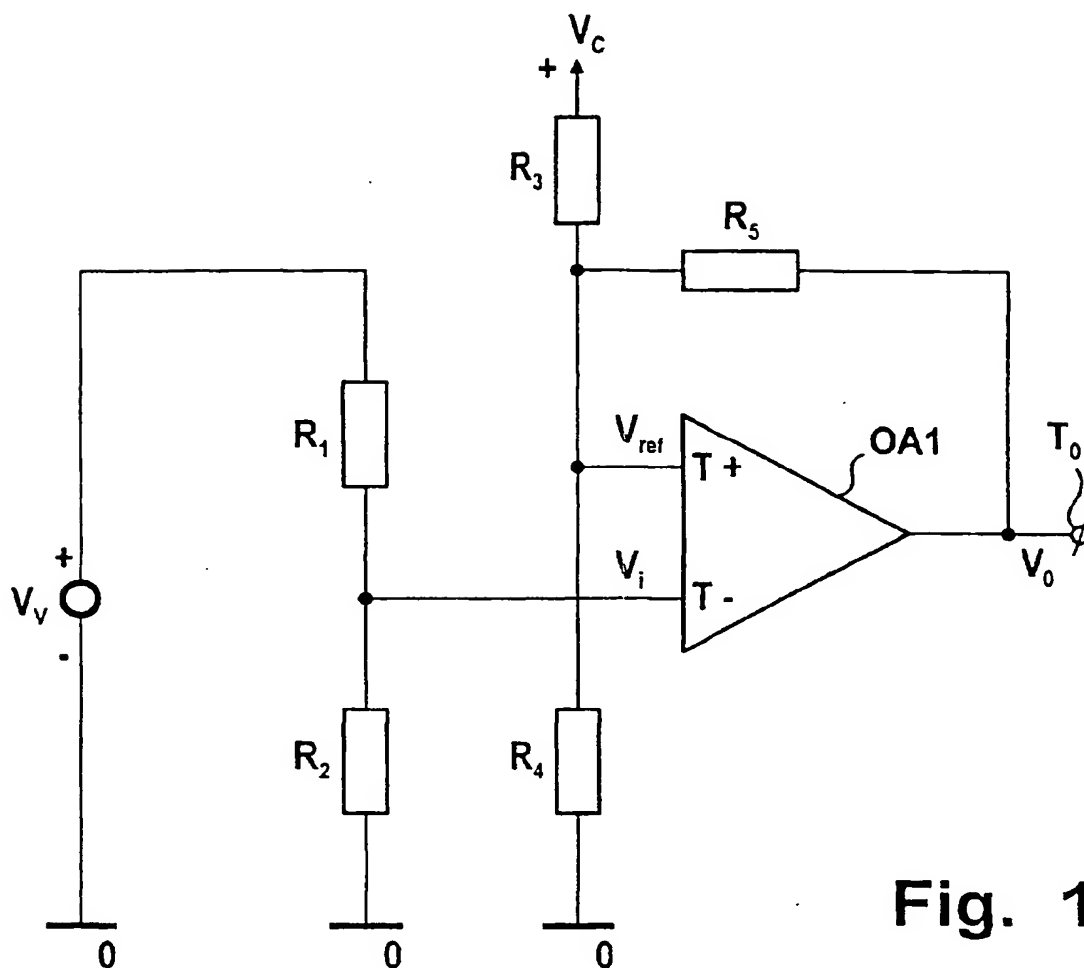


Fig. 1

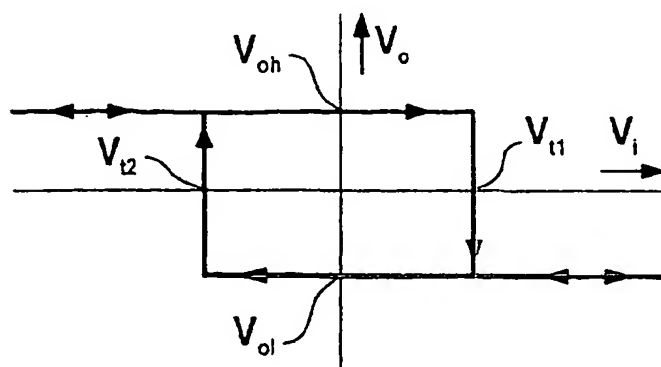
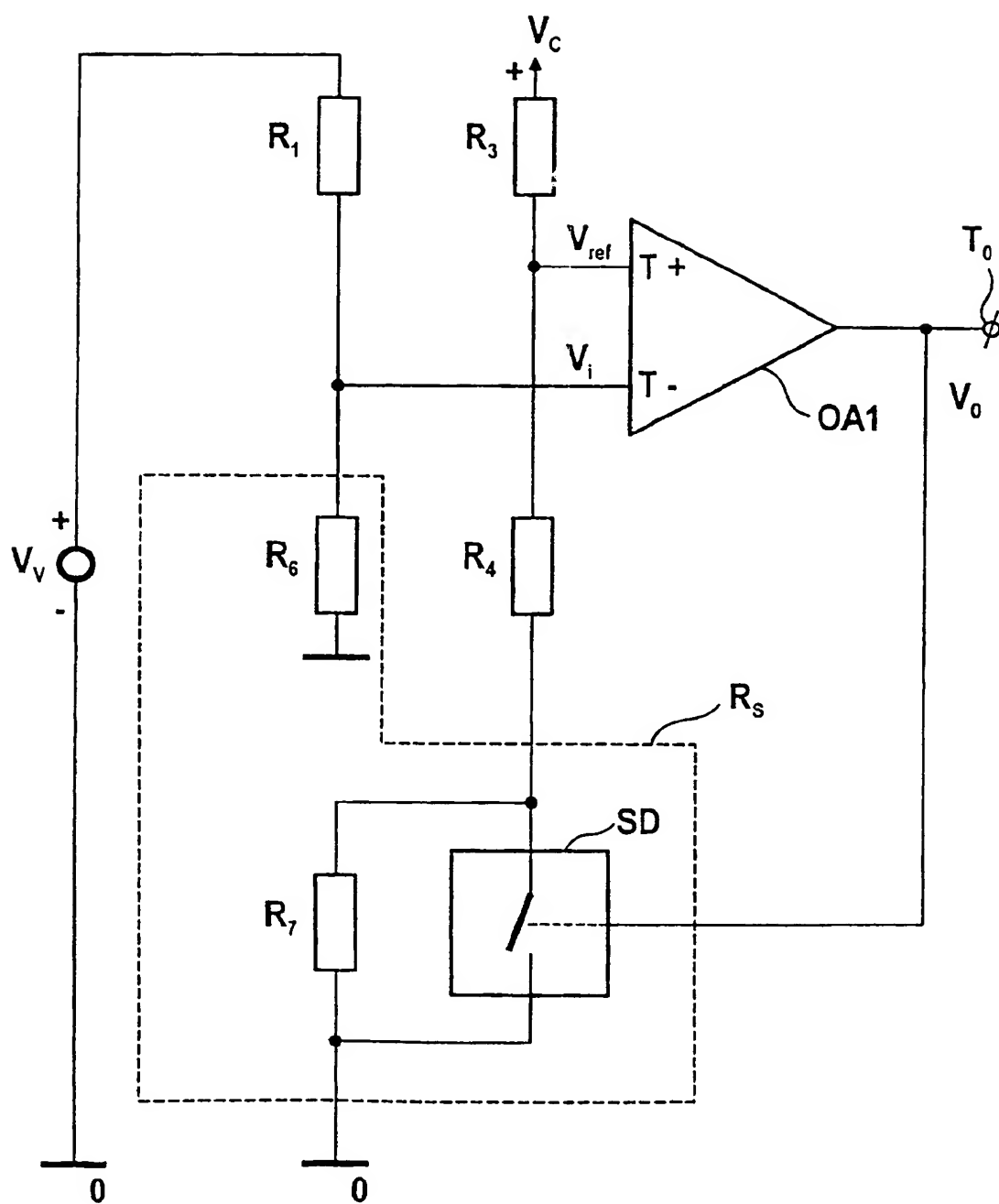


Fig. 2



**Fig. 3**

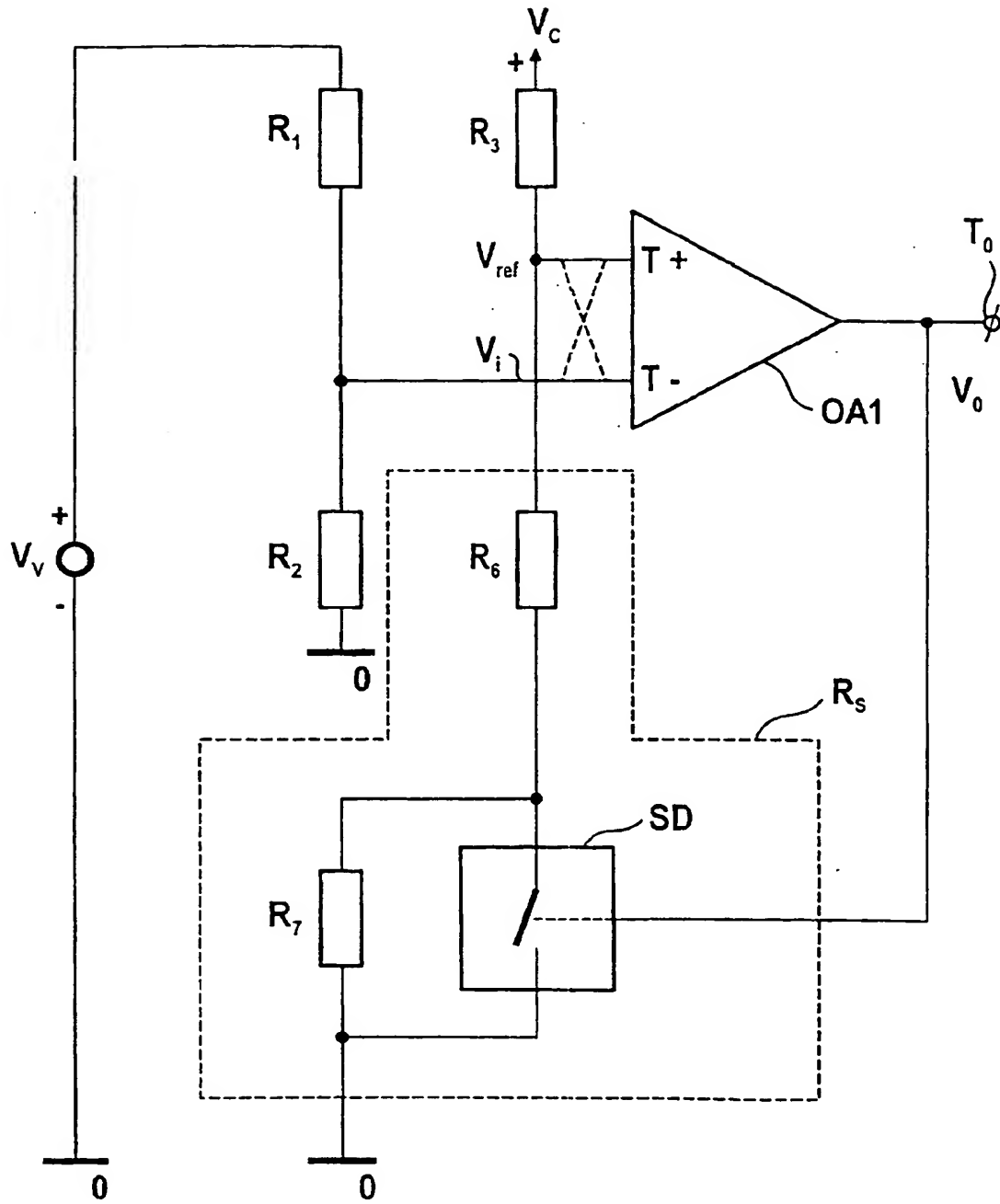


Fig. 4



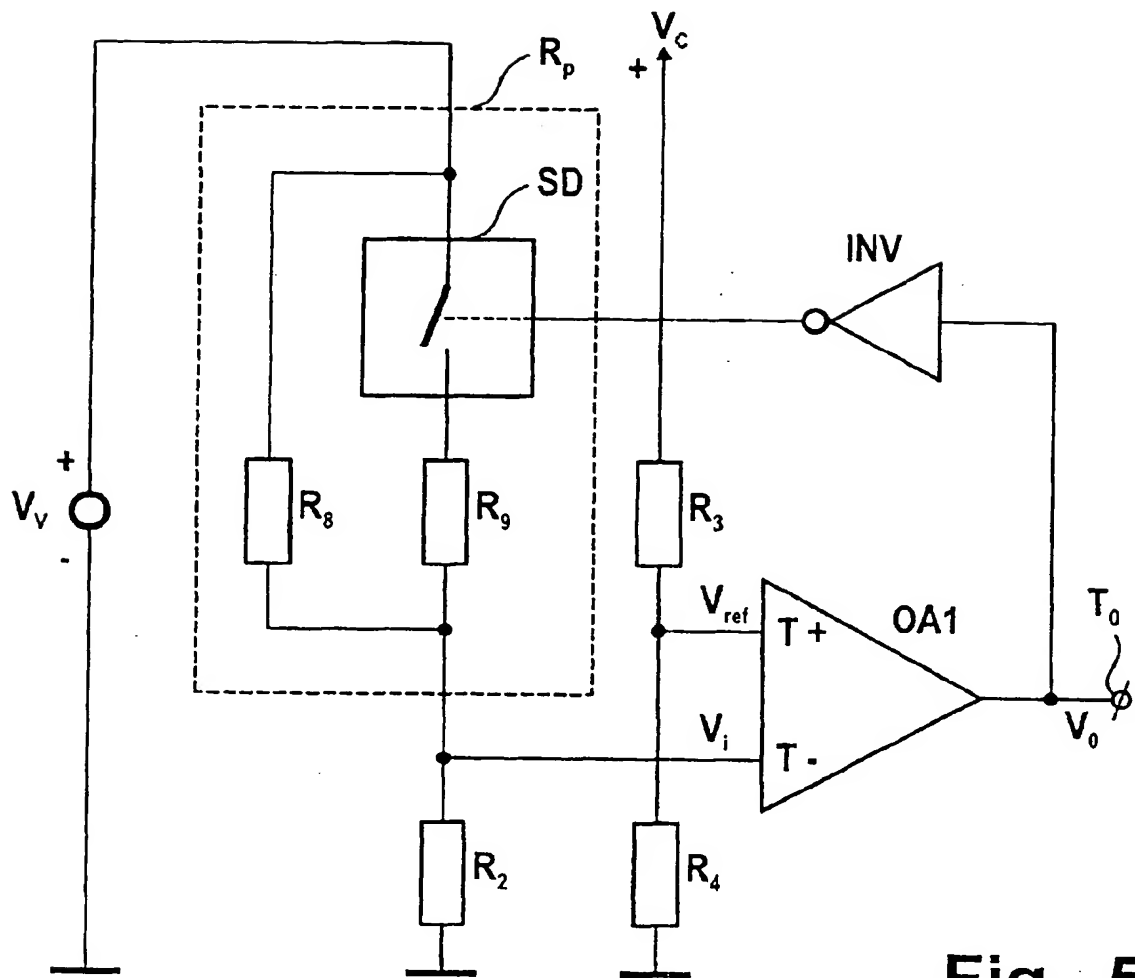


Fig. 5

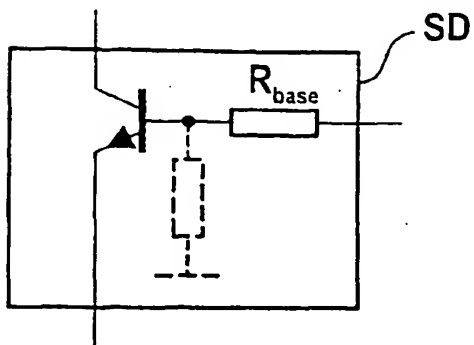


Fig. 10 A

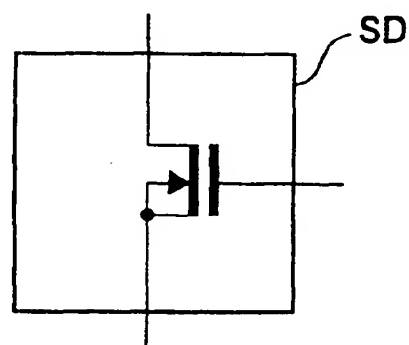


Fig. 10 B

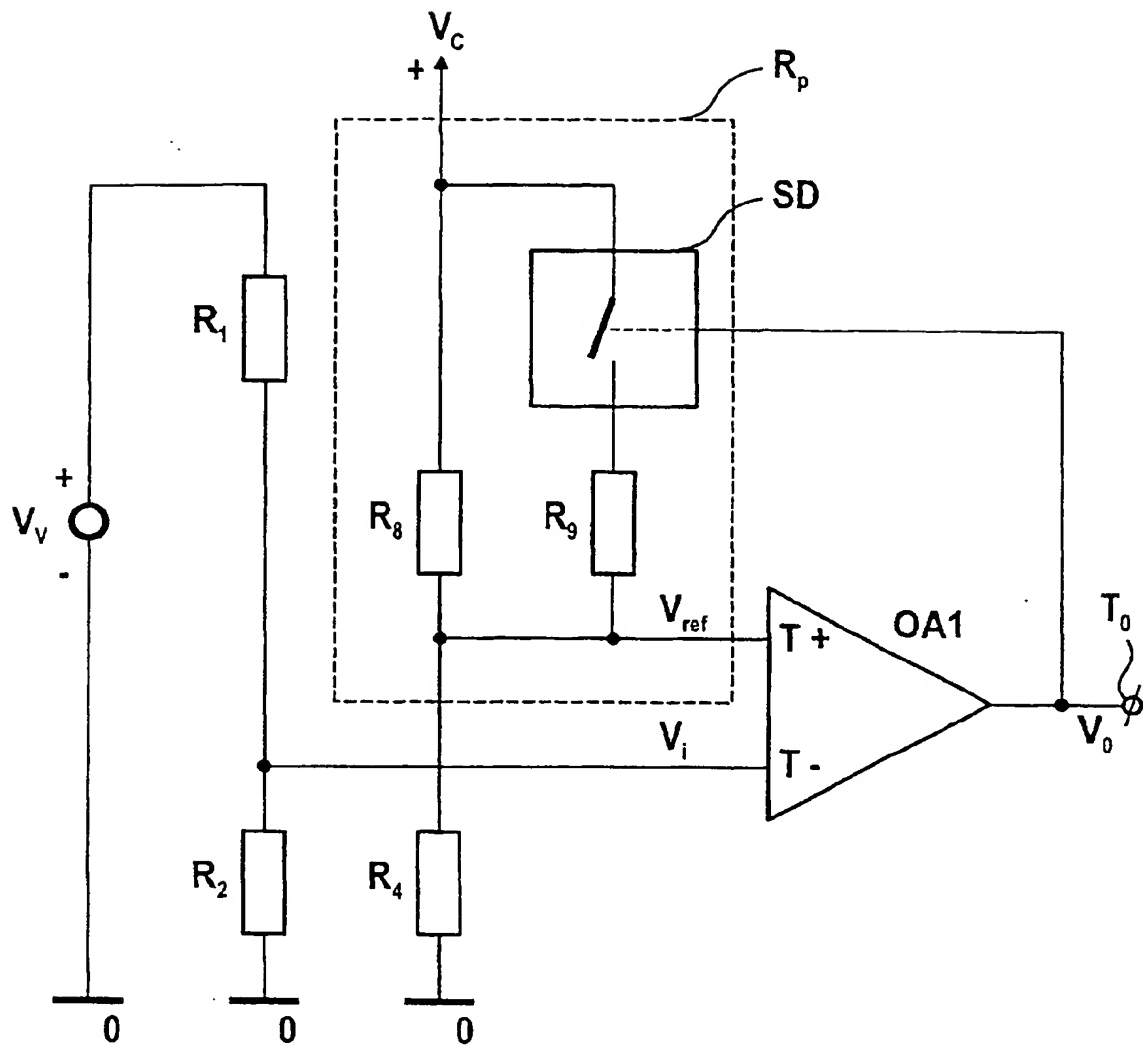


Fig. 6

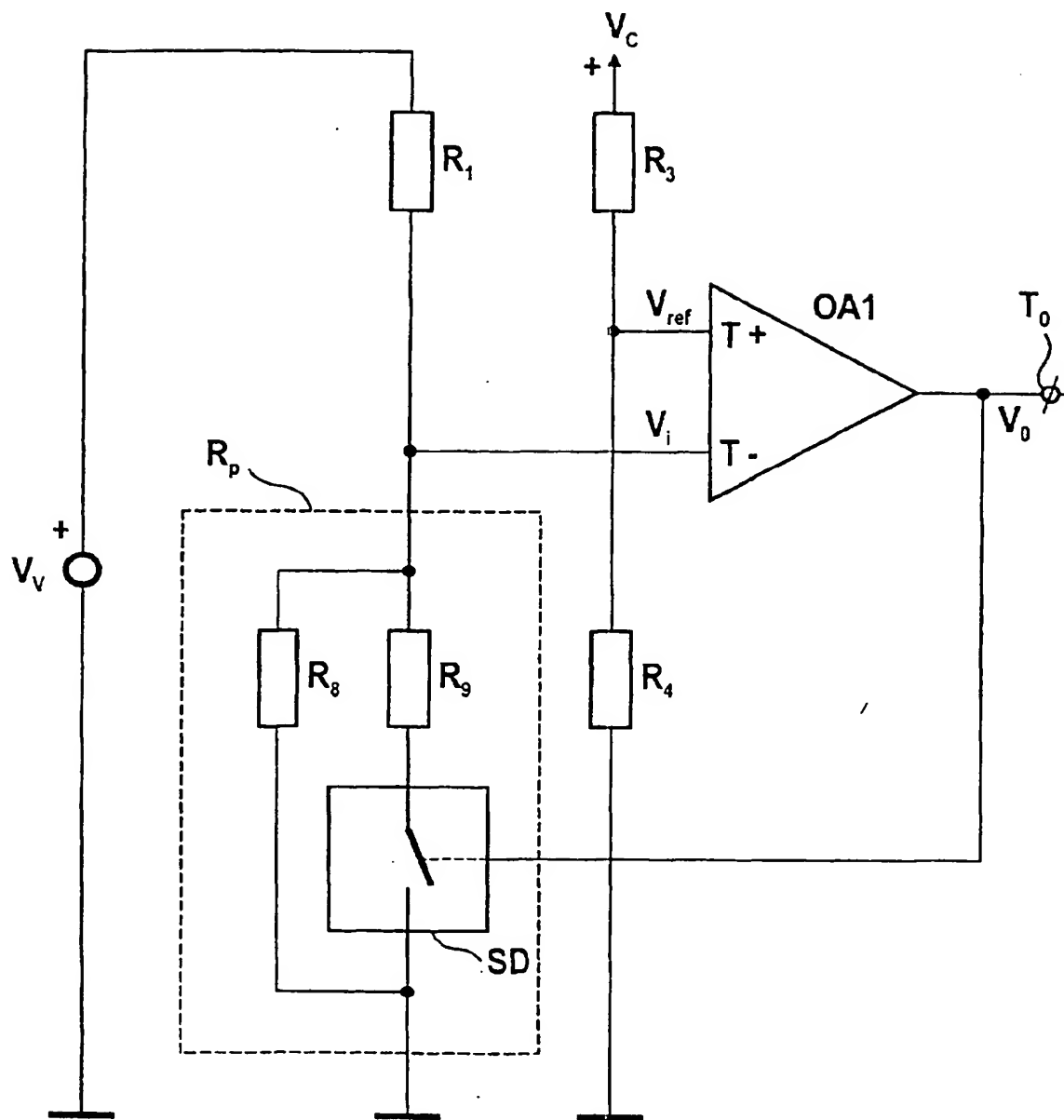


Fig. 7

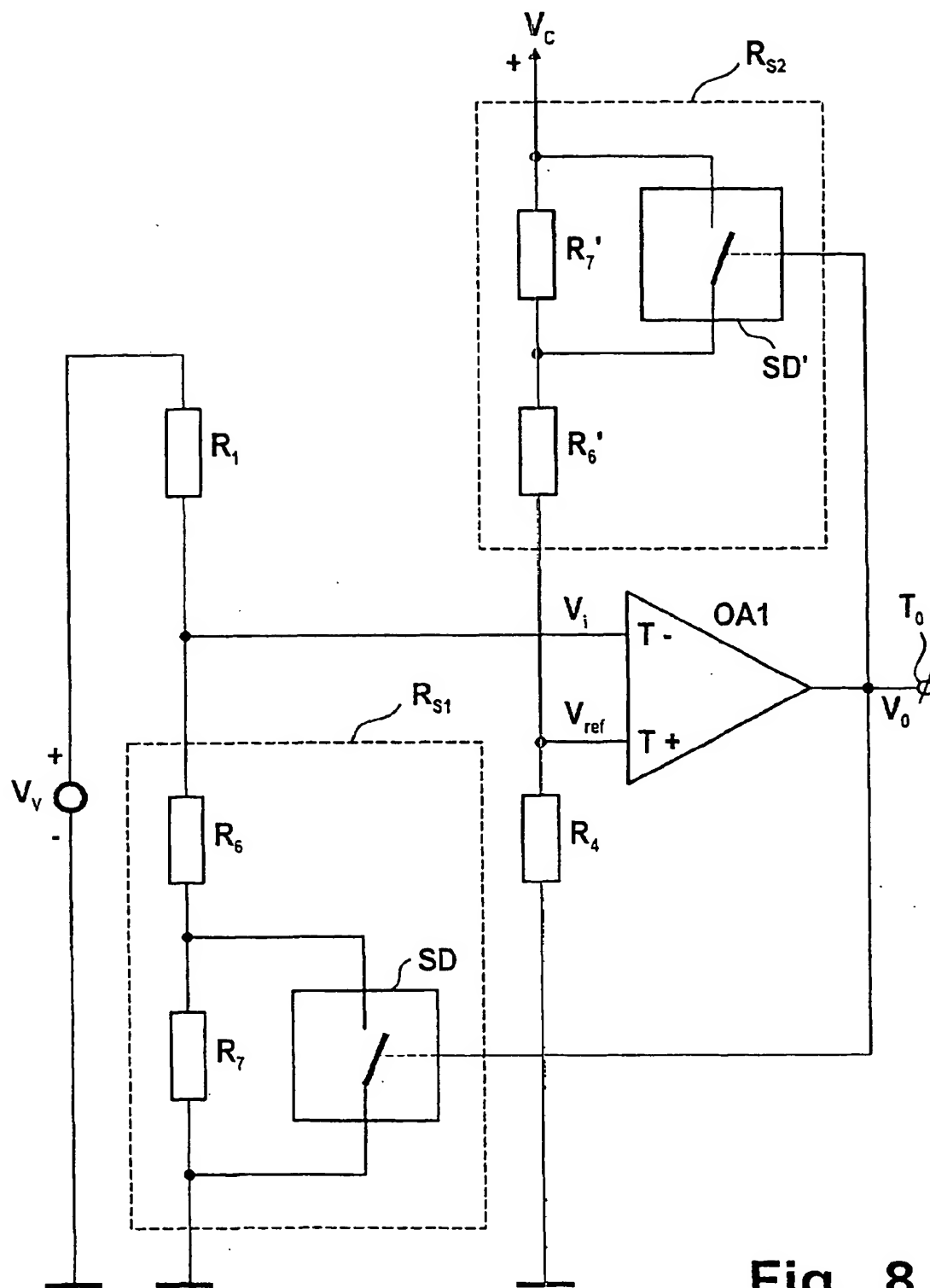


Fig. 8

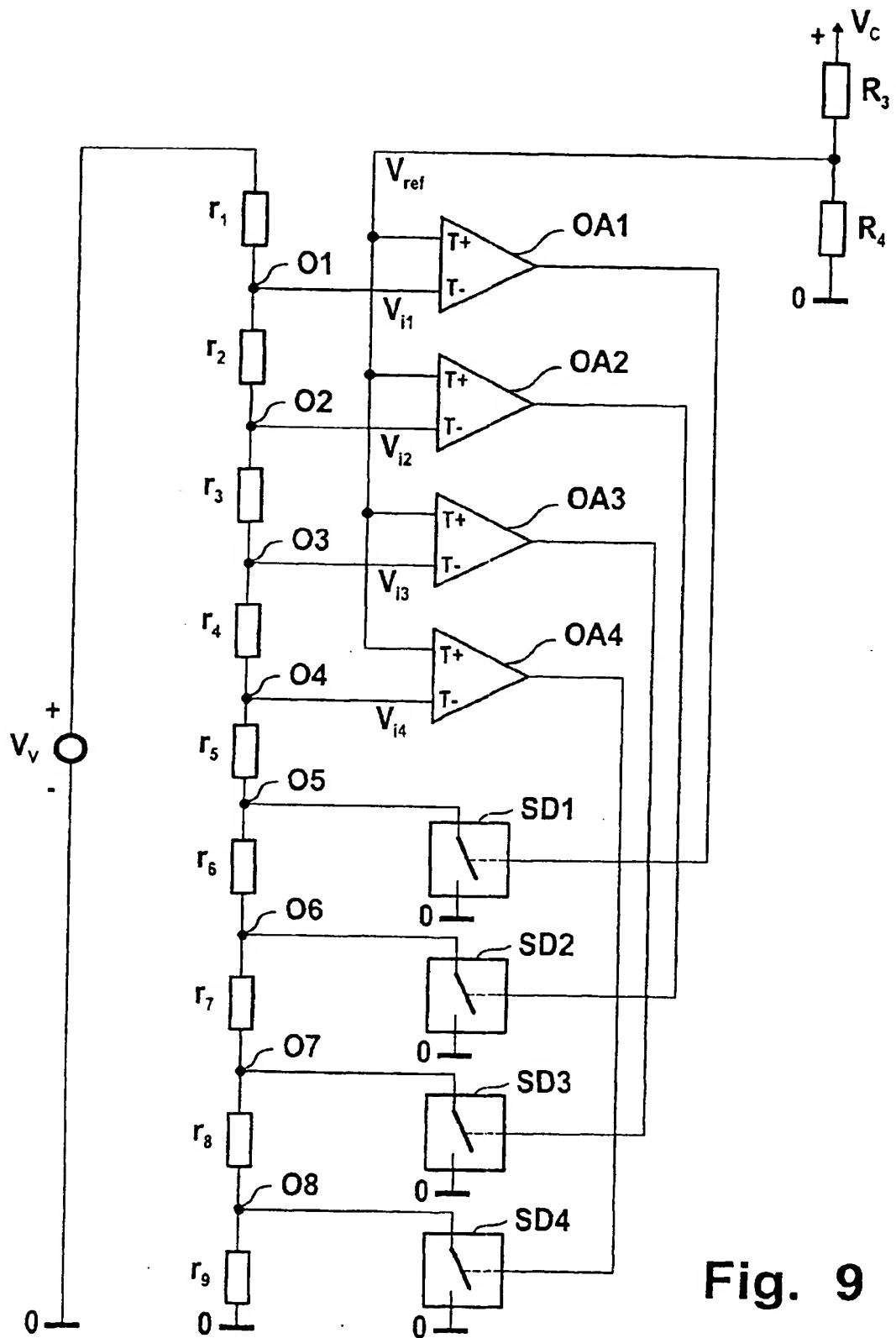


Fig. 9

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